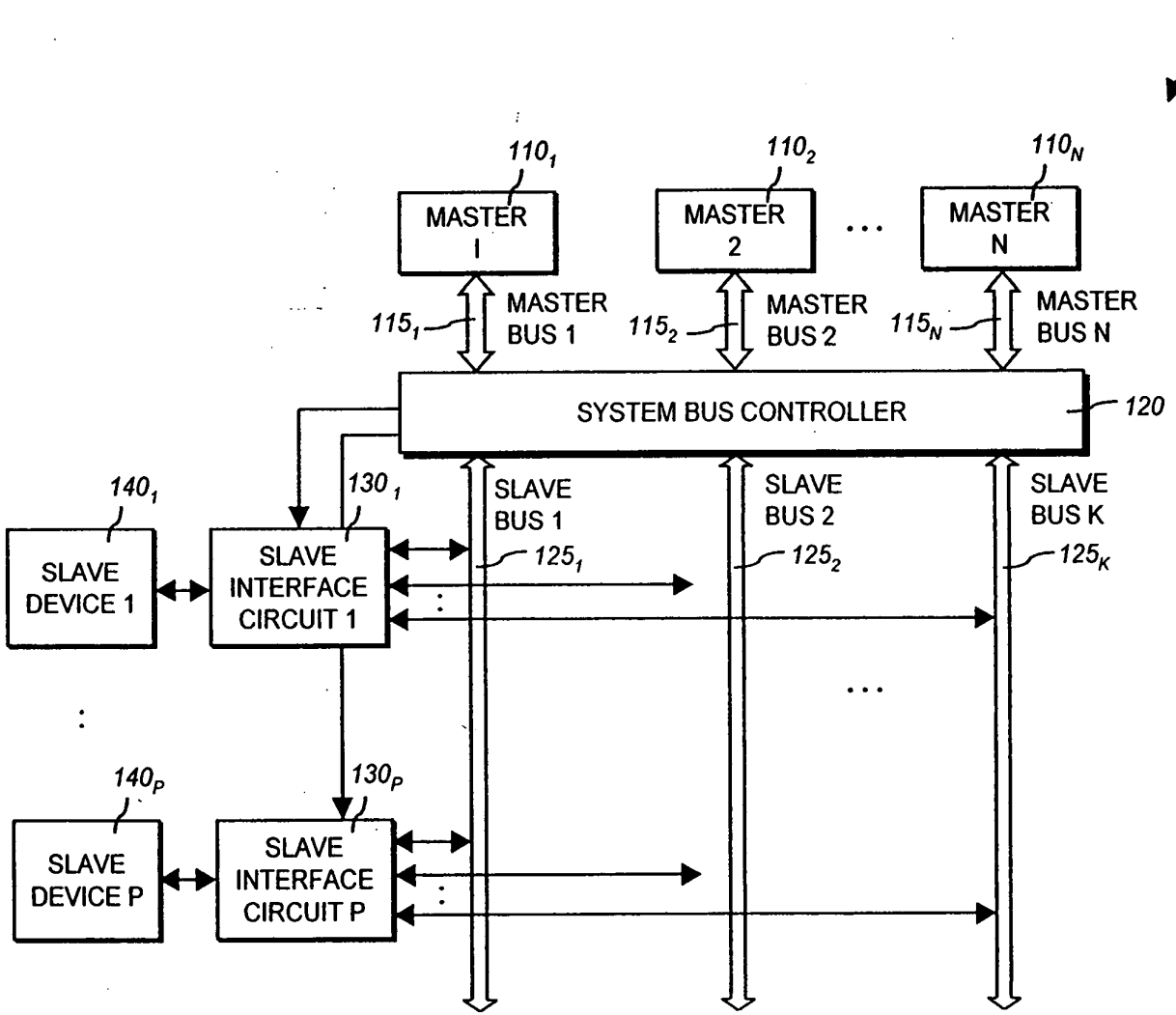
100
110₁
110₂
110N
MASTER 1
MASTER 2
MASTER N
115₁
MASTER BUS 1
115₂
MASTER BUS 2
115N
MASTER BUS N
SYSTEM BUS CONTROLLER
120
140₁
130₁
SLAVE DEVICE 1
SLAVE INTERFACE CIRCUIT 1
SLAVE BUS 1
SLAVE BUS 2
SLAVE BUS K
125₁
125₂
125K
140P
130P
SLAVE DEVICE P
SLAVE INTERFACE CIRCUIT P

FIG.1

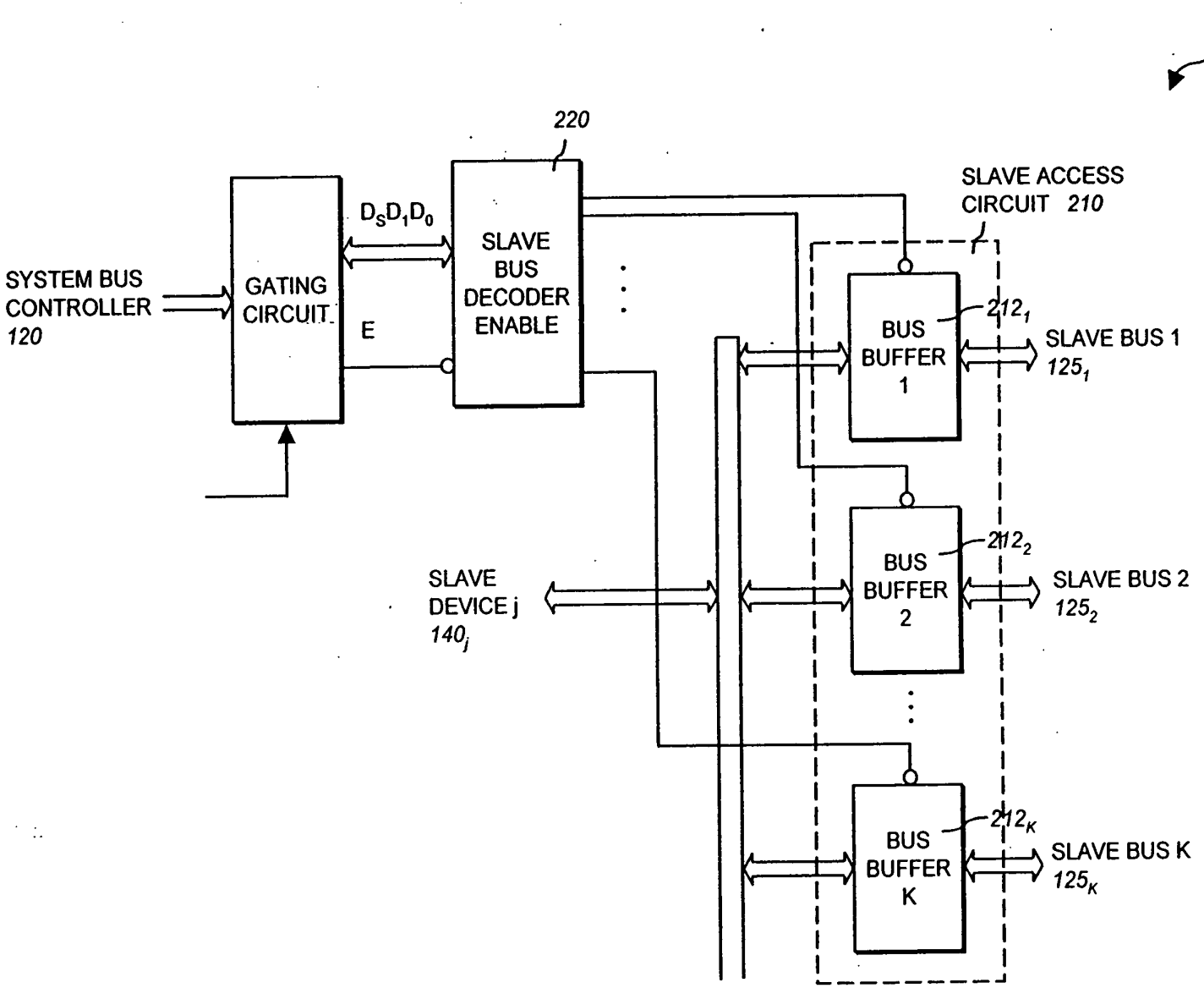
130j
220
SLAVE ACCESS CIRCUIT 210
SYSTEM BUS CONTROLLER 120
GATING CIRCUIT
DSD1D0
E
SLAVE BUS DECODER ENABLE
BUS BUFFER 1
2121
SLAVE BUS 1 1251
BUS BUFFER 2
2122
SLAVE BUS 2 1252
SLAVE DEVICE j 140j
BUS BUFFER K
212K
SLAVE BUS K 125K

FIG.2

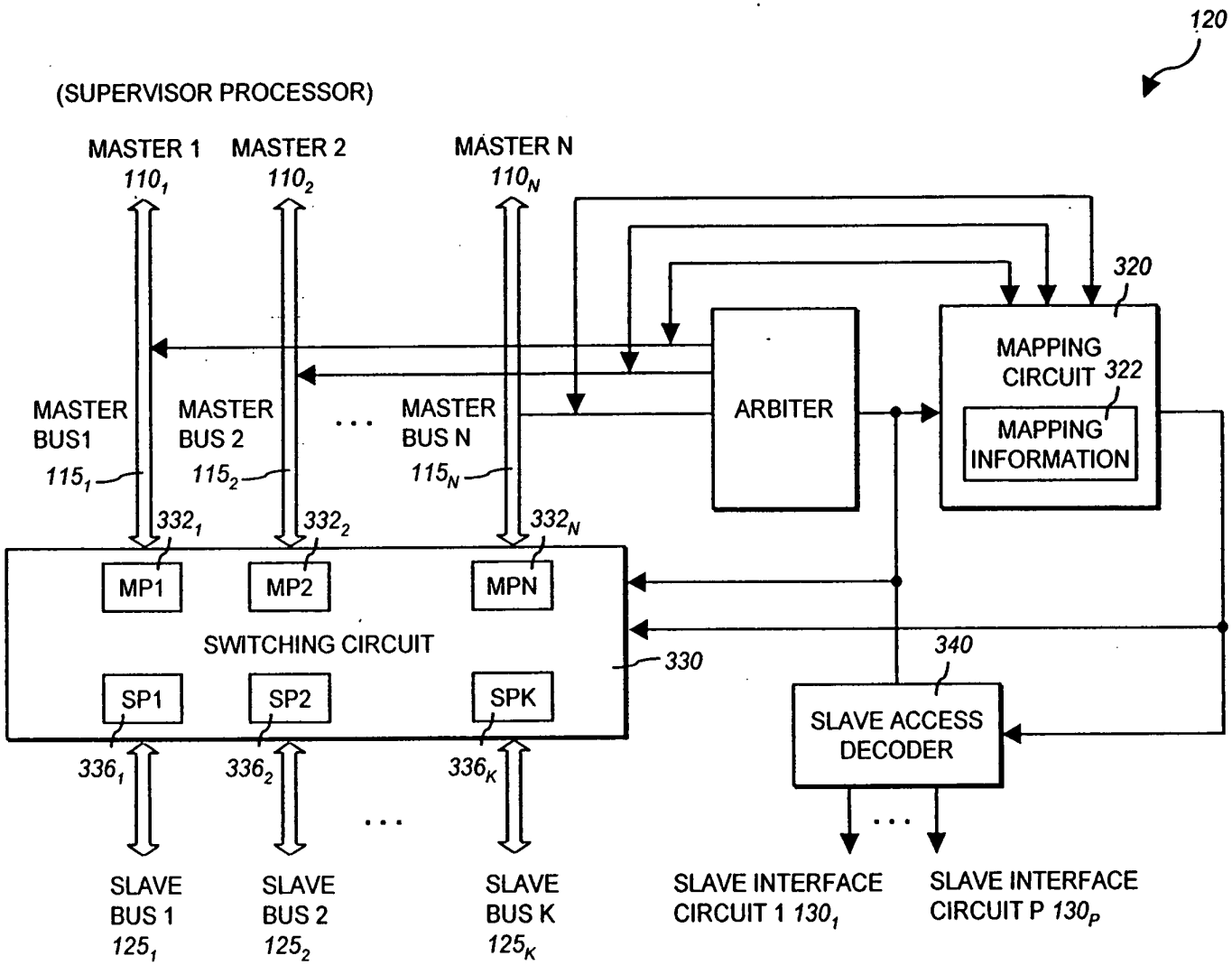
120
(SUPERVISOR PROCESSOR)
MASTER 1
110₁
MASTER 2
110₂
MASTER N
110N
320
MAPPING
CIRCUIT 322
MAPPING
INFORMATION
ARBITER
MASTER
BUS1
115₁
MASTER
BUS 2
115₂
MASTER
BUS N
115N
332₁
332₂
332N
MP1
MP2
MPN
SWITCHING CIRCUIT
330
340
SP1
SP2
SPK
SLAVE ACCESS
DECODER
336₁
336₂
336K
SLAVE
BUS 1
125₁
SLAVE
BUS 2
125₂
SLAVE
BUS K
125K
SLAVE INTERFACE
CIRCUIT 1 130₁
SLAVE INTERFACE
CIRCUIT P 130P

FIG.3

A	B	C	
00	00	XXXX	SLAVE 1
00	01	XXXX	SLAVE 2
	:		:
00	0(P-1)	XXXX	SLAVE P
	:		:
01	00	XXXX	SLAVE 1
01	01	XXXX	SLAVE 2
	:		:
01	0(P-1)	XXXX	SLAVE P
	:		:
0(L-1)	00	XXXX	SLAVE 1
0(L-1)	01	XXXX	SLAVE 2
	:		:
0(L-1)	0(P-1)	XXXX	SLAVE P
	:		:

FIG.4

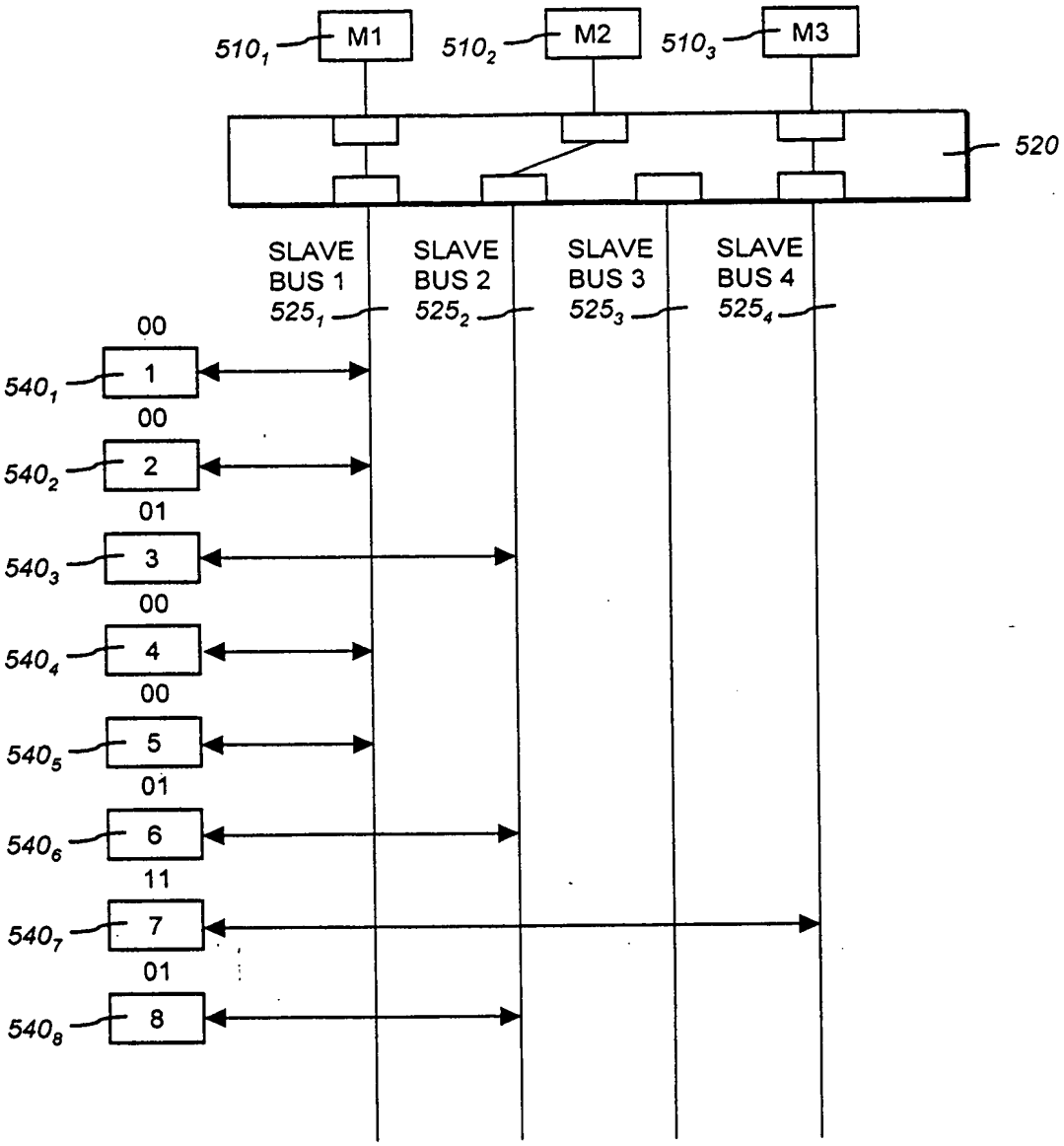
510₁
M1
510₂
M2
510₃
M3
520
SLAVE BUS 1
525₁
SLAVE BUS 2
525₂
SLAVE BUS 3
525₃
SLAVE BUS 4
525₄
00
1
540₁
00
2
540₂
01
3
540₃
00
4
540₄
00
5
540₅
01
6
540₆
11
7
540₇
01
8
540₈

FIG.5A

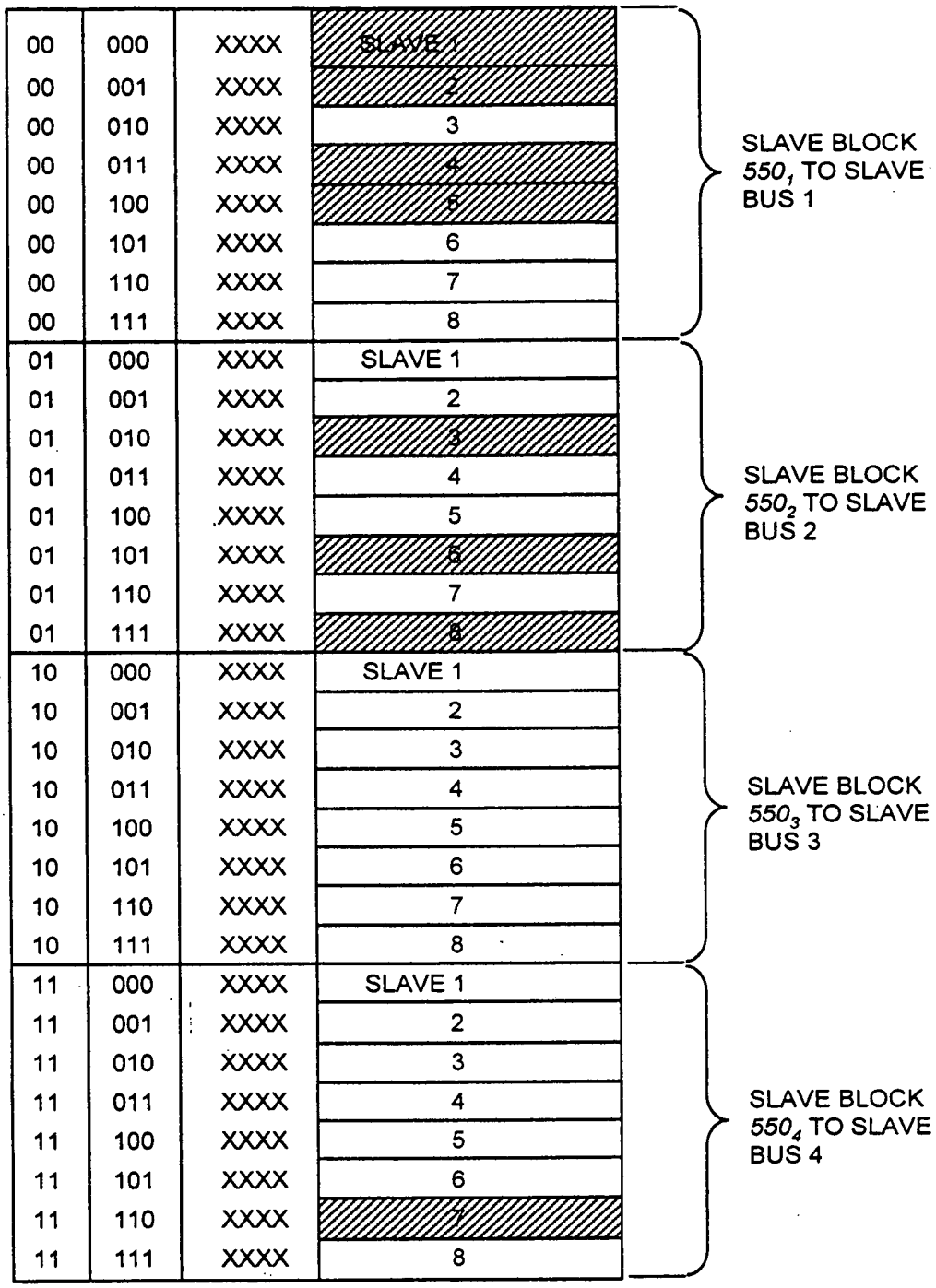
00 000 XXXX SLAVE 1
00 001 XXXX 2
00 010 XXXX 3
00 011 XXXX 4
00 100 XXXX 5
00 101 XXXX 6
00 110 XXXX 7
00 111 XXXX 8
SLAVE BLOCK 550, TO SLAVE BUS 1
01 000 XXXX SLAVE 1
01 001 XXXX 2
01 010 XXXX 3
01 011 XXXX 4
01 100 XXXX 5
01 101 XXXX 6
01 110 XXXX 7
01 111 XXXX 8
SLAVE BLOCK 550₂ TO SLAVE BUS 2
10 000 XXXX SLAVE 1
10 001 XXXX 2
10 010 XXXX 3
10 011 XXXX 4
10 100 XXXX 5
10 101 XXXX 6
10 110 XXXX 7
10 111 XXXX 8
SLAVE BLOCK 550₃ TO SLAVE BUS 3
11 000 XXXX SLAVE 1
11 001 XXXX 2
11 010 XXXX 3
11 011 XXXX 4
11 100 XXXX 5
11 101 XXXX 6
11 110 XXXX 7
11 111 XXXX 8
SLAVE BLOCK 550₄ TO SLAVE BUS 4

FIG.5B

	SLAVE DEVICE							
	1	2	3	4	5	6	7	8
	D_1D_0E	D_1D_0E	D_1D_0E	D_1D_0E	D_1D_0E	D_1D_0E	D_1D_0E	D_1D_0E
00 000	000	XX1	XX1	XX1	XX1	XX1	XX1	XX1
00 001	XX1	000	XX1	XX1	XX1	XX1	XX1	XX1
00 010	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
00 011	XX1	XX1	XX1	000	XX1	XX1	XX1	XX1
00 100	XX1	XX1	XX1	XX1	000	XX1	XX1	XX1
00 101	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
00 110	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
00 111	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
01 000	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
01 001	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
01 010	XX1	XX1	010	XX1	XX1	XX1	XX1	XX1
01 011	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
01 100	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
01 101	XX1	XX1	XX1	XX1	XX1	010	XX1	XX1
01 110	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
01 111	XX1	XX1	XX1	XX1	XX1	XX1	XX1	010
10 000	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
10 001	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
10 010	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
10 011	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
10 100	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
10 101	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
10 110	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
10 111	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
11 000	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
11 001	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
11 010	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
11 011	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
11 100	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
11 101	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1
11 110	XX1	XX1	XX1	XX1	XX1	XX1	110	XX1
11 111	XX1	XX1	XX1	XX1	XX1	XX1	XX1	XX1

FIG.5C